

first transistor and second low concentration source/drain regions of the second conductive type for the second transistor;

doping impurities of the second conductive type into the first and second source/drain regions of the second conductive type to form first high concentration source/drain regions of the second conductive type for the first transistor and second high concentration source/drain regions of the second conductive type for the second transistor;

doping impurities of the second conductive type by using a resist film, as a mask, having an opening in a region for forming the second transistor to form a low concentration second conductive type layer connecting the second low concentration source/drain regions; and

doping impurities of the first conductive type by using a resist film, as a mask, having an opening at a part of the second conductive type layer to form a semiconductor layer of the first conductive type below a gate electrode of the second transistor, wherein the semiconductor layer of the first conductive type parts the low concentration second conductive type layer.

REMARKS

On page 8, line 21, the paragraph has been rewritten to clarify the applicability of the invention. Support for such an amendment can be found, for example, on page 8 line 21.

The corrections on page 9, lines 22-23 and on page 11, lines 14-15 are supported by, for example, original claim 6. These corrections were made to make the terminology in the specification consistent with the claims and the remainder of the specification.

The correction on page 10, line 19 was made to correct a typographical error. The second-low concentration P-type source drain layer 14 is complementary to the second-low concentration N-type source drain layers 13 as shown in FIG. 3. Support for such a correction also can be found on page 10, lines 16-20.

On page 14, lines 1-6 have been rewritten to correct grammatical errors and to clarify the subject matter. Support for such a correction can be found on, for example, page 14 lines 1-6.

Claims 22-28 have been added, and are based on original claims 6-21. No new matter has been added.

Attached is a marked-up version of the changes being made by the current amendment.

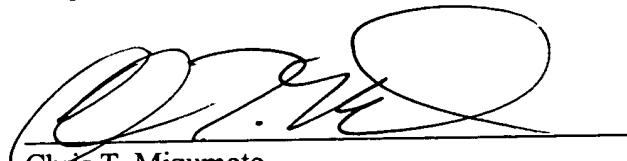
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125462M/HW

Applicant asks that all claims be examined. Please apply any other charges or credits to
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Respectfully submitted,

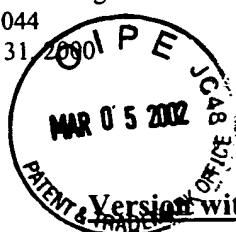
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TC 2300 MAIL ROOM

In the specification:

Paragraph beginning at page 8, line 21, has been amended as follows:

-- A method of manufacturing various MOS transistors composing the driver for driving a liquid crystal will be described below. The semiconductor of the present invention is applicable to various drivers such as a liquid crystal driver.--

Paragraph beginning at page 9, line 22 to page 10, line 15, has been amended as follows:

--Next, a first low concentration N-type [source] and P-type source/drain layers (hereinafter called an LN layer 10 and an LP layer 11) are formed using a resist film as a mask. That is, first, phosphorus ions for example are implanted into the superficial layer of the substrate at the acceleration voltage of approximately 120 KeV under the implantation condition of $8 \times 10^{12}/\text{cm}^2$ in a state that an area except an area where the LN layer is formed is covered with a resist film not shown so as to form the LN layer 10. Afterward, boron ions for example are implanted into the superficial layer of the substrate at the acceleration voltage of approximately 120 KeV under the implantation condition of $8.5 \times 10^{12}/\text{cm}^2$ in a state that an area except an area where the LP layer is formed is covered with a resist film (PR) so as to form the LP layer 11. Actually, each ion implanted as described above is thermically diffused after an annealing process (for example, for two hours in the atmosphere of N₂ of 1100°C) which is a postprocess to be the LN layer 10 and the LP layer 11.--

Paragraph beginning at page 10, line 16 to page 11, line 13, has been amended as follows:

--Next, as shown in Figs. 3, a second-low concentration N-type source drain layers (hereinafter called an SLN layer 13 [SLP layer 14]) are formed between the LN layers 10 using a resist film as a mask and a [surface] second-low concentration P-type source drain layers (hereinafter called an SLP layer 14) is formed between the LP layers 11 using a resist film as a mask. That is, first phosphorus ions for example are implanted into the superficial layer of the

substrate at the acceleration voltage of approximately 120 KeV under the implantation condition of $1.5 \times 10^{12}/\text{cm}^2$ in a state that an area except an area where the SLN layer is formed is covered with a resist film not shown so as to form the SLN layer 13 which ranges to the LN layer 10. Afterward, boron difluoride ions for example are implanted into the superficial layer of the substrate at the acceleration voltage of approximately 140 KeV under the implantation condition of $2.5 \times 10^{12}/\text{cm}^2$ in a state that an area except an area where the SLP layer is formed is covered with a resist film (PR) so as to form the SLP layer 14 which ranges to the LP layer 11. The impurity concentration of to the LN layer 10 and the SLN layer 13, or the LP layer 11 and the SLP layer 14 are set respectively substantially equal or one of them is higher then others.--

Paragraph beginning at page 11, line 14 to page 12, line 4, has been amended as follows:

--Further, as shown in Figs. 4, high concentration N-type [source] and P-type source/drain layers (hereinafter called an N+ layer 15 and a P+ layer 16) are formed using a resist layer as a mask. That is, first, phosphorus ions for example are implanted into the superficial layer of the substrate at the acceleration voltage of approximately 80 KeV under the implantation condition of $2 \times 10^{15}/\text{cm}^2$ in a state that an area except an area where the N+ layer is formed is covered with a resist film not shown so as to form the N+ layer 15 which ranges to the LN layer 10. Afterward, boron difluoride ions for example are implanted into the superficial layer of the substrate at the acceleration voltage of approximately 140 KeV under the implantation condition of $2 \times 10^{15}/\text{cm}^2$ in a state that an area except an area where the P+ layer is formed is covered with a resist film (PR) so as to form the P+ layer 16.--

Paragraph beginning at page 13, line 7 to page 14, line 6, has been amended as follows:

--That is, boron ions are similarly implanted into the superficial layer of the substrate at the acceleration voltage of approximately 50 KeV under a second implantation condition of $2.6 \times 10^{15}/\text{cm}^2$ in a state that an area except an area where the P-type layer is formed is covered with a resist film not shown so as to form the second P-type well 21 after boron ions for example are implanted into the P-type well 3 at the acceleration voltage of approximately 190 KeV under a first implantation condition of $1.5 \times 10^{13}/\text{cm}^2$ using a resist film not shown having its opening on an area where the N-channel MOS transistor is formed for normal resistance to voltage as a

mask. Also, phosphorus ions for example are implanted into the P-type well 3 at the acceleration voltage of approximately 380 KeV under the implantation condition of $1.5 \times 10^{13}/\text{cm}^2$ using a resist film (PR) having its opening on an area where the P-channel MOS transistor is formed for normal resistance to voltage as a mask so as to form the second N-type well 22. In case a generator of the acceleration voltage of approximately 380 KeV is not provided, [a double charging method in which phosphorus ion is implanted at the acceleration voltage of 190 KeV under the implantation condition of $1.5 \times 10^{13}/\text{cm}^2$ and then phosphorus ion is implanted at the acceleration voltage of 150 KeV under the implantation condition of $4.0 \times 10^{12}/\text{cm}^2$ may be also adopted.] A double charging method in which bivalent phosphorus ion is implanted at the acceleration voltage of 190 keV under the implantation condition of $1.5 \times 10^{13}/\text{cm}^2$ may be also adopted. Subsequently phosphorus ion is implanted at the acceleration voltage of 150 keV under the implantation condition of $4.0 \times 10^{12}/\text{cm}^2$.